High-Efficiency 1-, 2-, and 4-W Class-B FET Power Amplifiers

JOHN R. LANE, MEMBER, IEEE, RONALD G. FREITAG, MEMBER, IEEE, HYO-KUN HAHN, MEMBER, IEEE, JAMES E. DEGENFORD, FELLOW, IEEE, AND MARVIN COHN, FELLOW, IEEE

Abstract — *X*-band GaAs FET amplifiers utilizing the higher efficiency of class-B operation have been designed and fabricated. This paper describes the design of these amplifiers and includes the results of a computer time-domain simulation of one of the topologies, which gives insight into the harmonic content of the output currents in different branches of the FET and amplifier circuit. The performance is presented of 1-W single-ended, 2-W push-pull, and 4-W dual push-pull amplifiers having state-of-the-art power-added efficiencies of 45 percent, 40 percent, and 35 percent, respectively, in a 1-GHz bandwidth, with associated gains of 5.8 dB, 5.4 dB, and 5.0 dB. Data are given for 15-unit lots of the 1-W and 2-W units to show the consistency of their performance [1]. In addition to output power and efficiency data, this paper includes information on AM-to-PM conversion, second-harmonic generation, and intermodulation products.

I. Introduction

CLASS-B AMPLIFICATION is defined as that mode in which the active device amplifies during one-half the input signal's period and is idle the remaining time. This mode of operation as applicable to microwave power FET's has several important advantages over class-A biasing for many applications, such as in an array of transmit/receive radar modules [2]. The higher theoretical drain efficiency of class B, a maximum of 78.5 percent versus 50 percent for the class-A full-wave mode, results in a significant lowering of dc input power and heat dissipation. For an array design, this translates into large reductions in prime power and an easing of thermal design considerations. Also, the self-turn-on and -turn-off characteristic of class-B amplifiers under pulsed operation simplifies or even eliminates the bias synchronization problem inherent in class-A amplifiers.

The transconductance of almost all microwave power GaAs FET's is fairly constant over most of the gate-to-source input voltage range but decreases rapidly as the channel pinches off; this includes the FET's (Fig. 1) used in the amplifiers reported here. This degrades both the small-signal and power gain of an amplifier when attempts are made to bias it at or very near pinchoff.

As a reasonable compromise between high efficiency and gain over a large dynamic range, the amplifiers in this paper were biased to a quiescent drain current value of $I_{DQ} \simeq 10$-percent I_{DSS}. Hence, they do not operate purely as class B, but to a close approximation where the conduction angle is not much larger than 180°; this is to be distinguished from general class-AB operation, defined as having a conduction angle anywhere between 180° and 360°. As an illustration of this operating mode, measured curves of RF power output (P_{OUT}), applied dc power (P_{DC}), dissipated power (P_{DISS}), and power-added efficiency (η_{PA}) versus RF input power (P_{IN}) are plotted in Fig. 2 for a typical 1-W high-efficiency amplifier biased at 10-percent I_{DSS}. At zero RF drive, P_{DC} and P_{DISS} are not zero, which would correspond to true class B, but they are a small fraction of the values they would have for class-A operation.

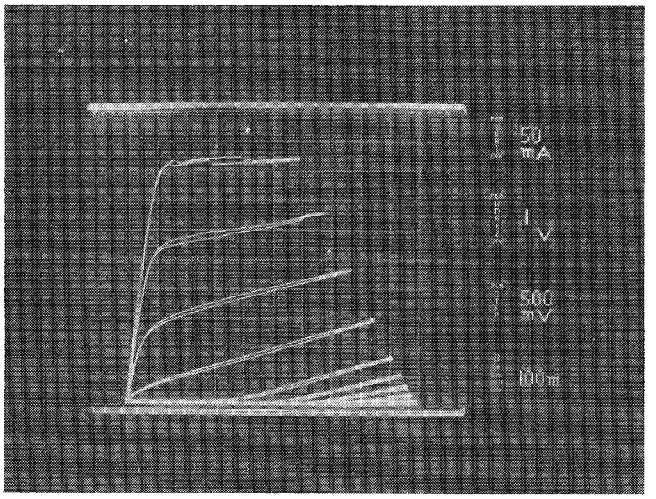


Fig. 1. $i-v$ curve of Fujitsu FLK 102XV GaAs FET.

II. FET Device Characteristics

The FET used in all the amplifiers was the Fujitsu FLK 102XV, used in chip form for size considerations and to allow the input matching scheme described next. The 2400-μm-periphery device employs plated-through source vias for bondless source grounding and good heat-sinking. These FET's were presorted by the manufacturer into groups having pinchoff voltages matched to ± 0.05 V. Nominal I_{DSS} was 400 mA and the nominal pinchoff voltage (at $V_{DS} = 5$ V) was -2.0 V. The selection process

Manuscript received April 8, 1986; revised July 1, 1986. This work was supported in part by AFWAL under Contract F33615-83-C-1058 and by NRL under Contract N00014-84-C-2411.

The authors are with the Westinghouse Electric Corporation, P.O. Box 1521 Baltimore, MD 21203.

IEEE Log Number 8610547.

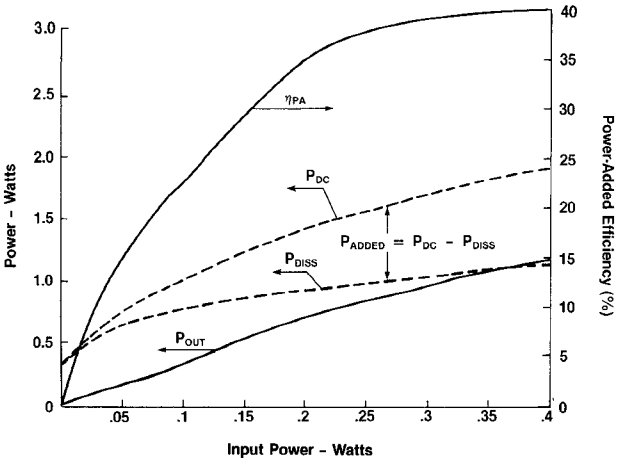


Fig. 2. Measured power characteristics of a high-efficiency FET amplifier biased at 10-percent I_{DSS}.

was judged to more than offset the reworking and tuning necessary if unsorted FLK 102XV's had been used, especially in the case of the push-pull amplifiers.

Eight individual FLK 102XV's were characterized at 9.7 GHz at both small-signal and rated power levels using loss-corrected tuner measurements. The average chip output power, gain, and power-added efficiency were 30.8 dBm, 6.0 dB, and 48 percent. Bias conditions were $V_D = 8.5$ V, $I_{DQ} = 40$ mA ($\simeq 10$ percent I_{DSS}), and $V_g = -2.0$ V to -2.5 V (depending on the pinchoff voltage group).

III. FET Matching Circuit

A major goal of this effort was the flatness of both output power and efficiency in the 9.2–10.2-GHz band. Thus, the tradeoff of increasing the number of tuning elements at the gate and drain of the FET to give flatter response versus the additional loss introduced was a major concern. Obviously, the efficiency is reduced more by a given amount of loss in the output than in the input.

The averaged small-signal input model of the FLK 102 at 10-percent I_{DSS} quiescent bias and under conjugate output power match conditions was 2.5 Ω in series with 1.8 pF, giving an input Q of 3.7 at 9.7 GHz. This small-signal input Q was about twice as high as the Q under class-A bias, since the gate–source capacitance at 10-percent I_{DSS} ($V_{GS} \simeq -2.0$ V) was roughly half that at 50-percent I_{DSS} ($V_{GS} \simeq -1.0$ V). The direct access to the gate pads of the FLK 102 chips made the following input matching scheme possible (illustrated in Fig. 3 for the 1-W design): bond wires were connected from the outermost gate pads to RF ground through 5-pF dc-blocking chip capacitors, parallel resonating the FET's input capacitance. This converted and increased the 2.5-Ω series input resistance to its parallel equivalent by a maximum factor of $(Q_{in}^2 - 1)$, with Q_{in} given below. A series L/shunt C transformer section then achieved the rest of the input match to a 50-Ω source with satisfactory flatness.

Critical for this input matching approach was the necessity of a gate shunt-resonating inductor having low loss: since $Q_{in}^{-1} = Q_{INDUCTOR}^{-1} + Q_{FET}^{-1}$, any losses in the inductor circuit would lower the $(Q_{in}^2 - 1)$ parallel resonance factor, thereby 1) narrowing the input bandwidth and 2) reducing the gain by absorbing input power. The short (~ 0.012 in long) shunt bond wire inductances needed were assumed to have low series resistance, and initially so were the 5-pF blocking caps. First results on the 4-W amplifiers showed good output power but narrow bandwidth, low gain, and low power-added efficiency, implying high input losses. This led to measurement of the blocking caps and the discovery, through DeLoach resonance tests of the original 5-pF chips, that the equivalent series resistance of these high-dielectric-constant ($\epsilon_R > 400$) capacitors was 1.3 Ω, giving a very low $Q_{cap} = 2.5$. Because the blocking capacitor and bond wire inductor on each side of the FET were in series, $Q_{CAP} = Q_{INDUCTOR}$, and significant loss could be expected at the FET input. Lower ϵ_R ($\simeq 110$) chip caps were obtained and tested to have less than 0.2-Ω series resistance; they restored the gain and efficiency of the gate-shunt-resonanted FET.

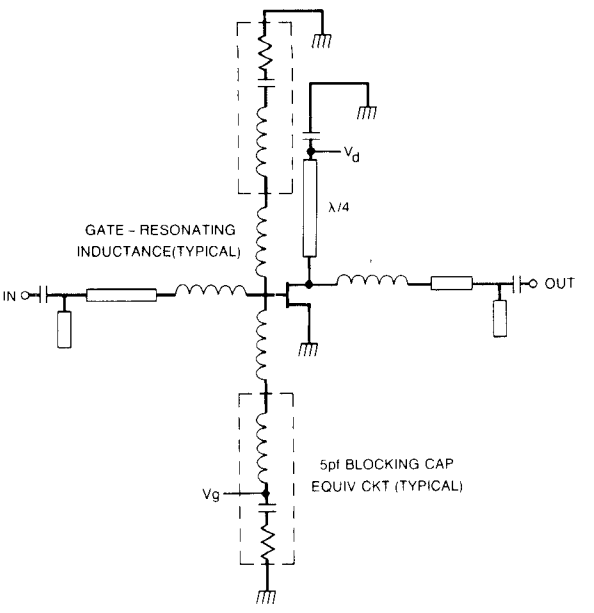


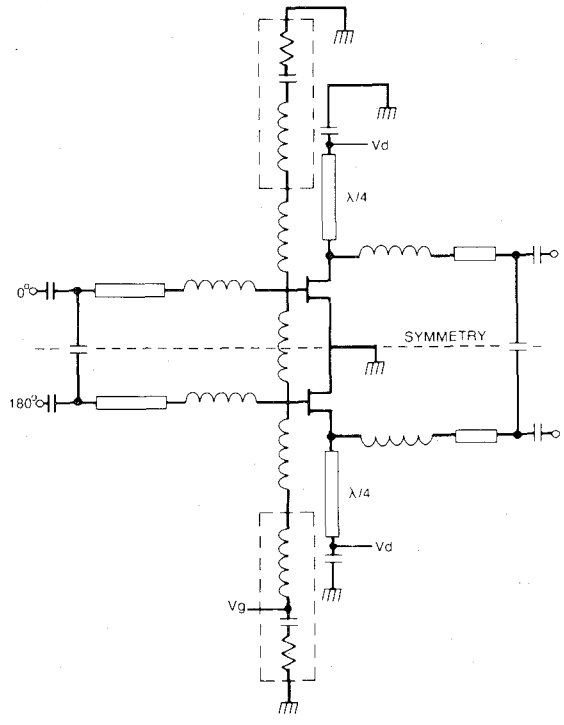
Fig. 3. Single-ended 1-W FET amplifier matching circuit.

Load-pull tests on the FLK 102XV indicated a Q of 1.2 for its equivalent output circuit, where the drain current was 10-percent I_{DSS} quiescent and 50-percent I_{DSS} under RF drive at approximately 1-W output. Accordingly, only a series L/shunt C section was needed for matching the drain, minimizing the power loss caused by finite tuning element Q's.

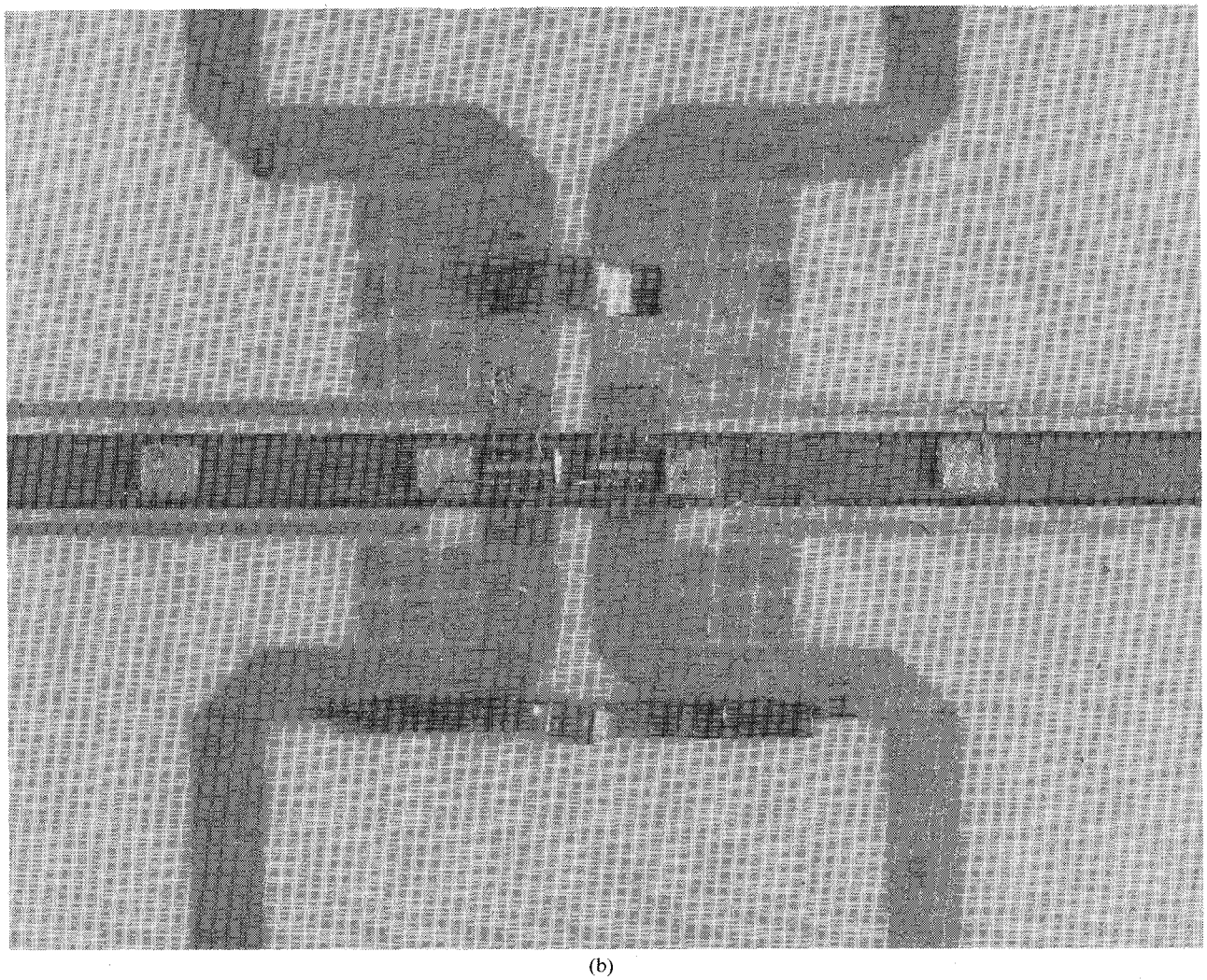
IV. 1-, 2-, and 4-W Amplifier Topologies

A. 1-W Single-Ended Amplifier

The 1-W single-ended amplifier used one FLK 102XV with matching described as above. The series L/shunt C sections were realized in 0.025-in alumina microstrip by series lengths of transmission line and shunt open stubs, respectively, with allowances made for bond wire inductances. Drain bias was delivered by 90-Ω shorted quarter-wavelength (at 9.7 GHz) stub pairs; at the second



(a)



(b)

Fig. 4. Two-watt push-pull amplifier. (a) Schematic. (b) Fabricated circuit.

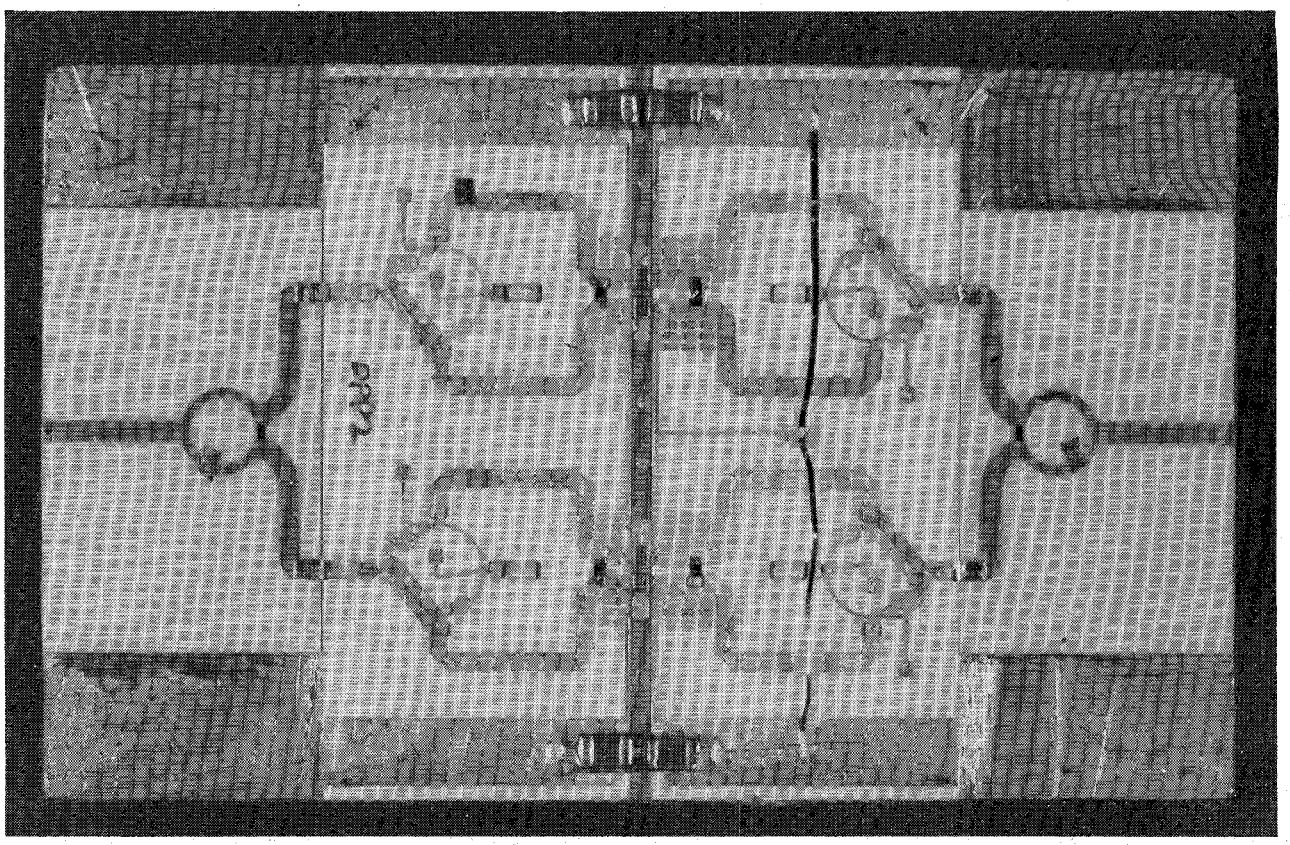


Fig. 5. Four-watt dual push-pull amplifier.

harmonic of the amplified signal, these stubs presented a low impedance to reflect second harmonic back into the drain. Experiments had shown an increase in output power of up to 5 percent from this effect. However, no specific second-harmonic tuning was done.

B. 2-W Push-Pull Amplifier

To obtain 2 W of output power, two of the FET's were combined. This was done in a push-pull configuration (Fig. 4) using 0°–180° hybrid splitters (shown as part of Fig. 5). This hybrid design, which is based on an approach described earlier by March [3], was implemented here in microstrip and modified for increased bandwidth. The insertion loss of the hybrids was less than 0.5 dB in the 9.2–10.2-GHz band, and the phase difference between the output ports was $180° \pm 2°$.

Since the hybrids combined the active devices antiphase, the virtual ground symmetry between them permitted the combination and reduction of some matching circuitry. First, the separate gate-resonating inductance bonds on the common side of the two FET's were replaced by one FET-to-FET gate bond across the symmetry line, eliminating two of the dc-blocking capacitors. The gates of the FET pair thus became dc-common, necessitating good pinchoff voltage matching as described in Section I. Also, the input and output shunt-open tuning stubs were replaced by beam-lead capacitor chips bonded between the antiphase input/output transmission lines. Quarter-wave drain bias stubs were still used for second-harmonic reflection.

C. 4-W Dual Push-Pull Amplifier

A 4-W dual push-pull topology was obtained by paralleling a pair of the 2-W amplifiers through *X*-band Wilkinson power splitters that had 0.2-dB dissipative loss each. The complete 4-W amplifier is shown in Fig. 5. The slight tuning that is evident was done to equalize the electrical lengths of the two 2-W halves; note that the circuitry around the individual FET's is identical. Reductions in both this amplifier's size and the power dissipated in the interconnecting 50-Ω lines can be realized in future versions.

V. Time-Domain Amplifier Simulation

The theoretical pure class-B half sine wave output of an amplifier operated well below its active device's cutoff frequency gives a second-harmonic level only 7 dB below the fundamental level. Since the amplifiers here were operated slightly class AB, it was expected that the second-harmonic level would be less than −7 dBc, but not nearly as low as was observed among measured units (Section VI). While the average measured second-harmonic level of less than −48 dBc at rated power seen in the single-ended amplifiers was a desirable characteristic, the causes of such suppression needed to be explained. Direct measurement of current and voltage waveforms at various points in a

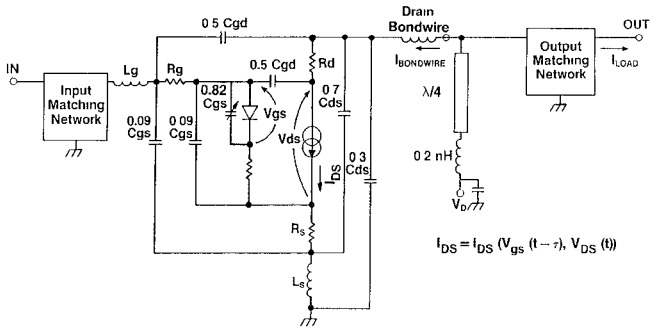


Fig. 6. Simulated 1-W amplifier circuit and FET model.

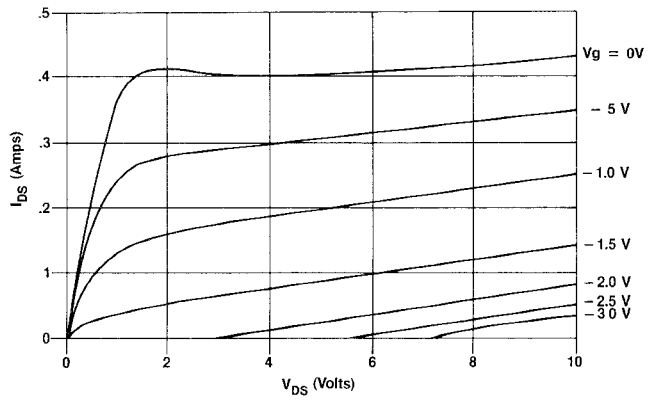


Fig. 7. Modeled $i-v$ curve of Fujitsu FLK 102XV GaAs FET.

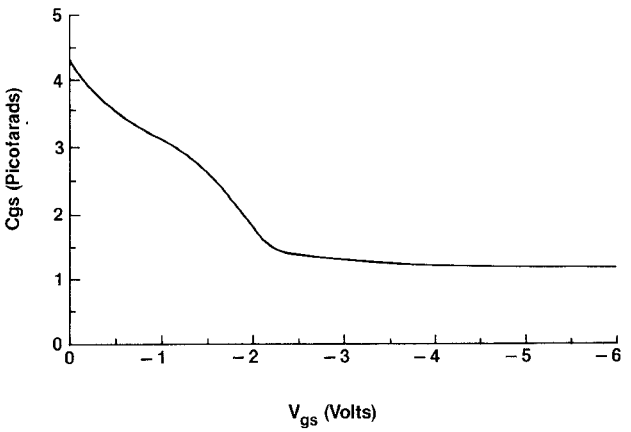


Fig. 8. Measured gate–source capacitance of Fujitsu FLK 102XV.

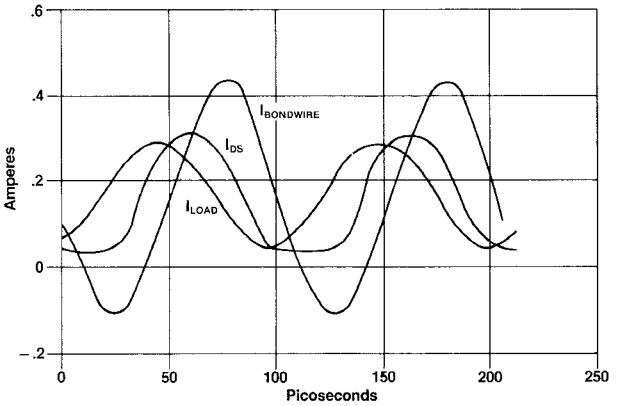


Fig. 9. Current waveforms in simulated circuit (P_{OUT} = 25.5 dBm).

microwave amplifier is impossible, so a time-domain simulation of the single-ended 1-W topology was done, using WATAND software (a University of Waterloo package) run interactively on a VAX 780 computer. With this simulation the relative levels of the fundamental and harmonics at nodes in the amplifier circuit and even in the FET model itself could be compared.

Fig. 6 shows the model of a Fujitsu FLK 102XV FET embedded in the 1-W single-ended matching circuits. This model includes two major nonlinearities. First (Fig. 7), the nonlinear transconductance (g_m) as a function of V_{GS} and V_{DS} is described by the modeled $i-v$ curve (compare with the measured $i-v$ curve of Fig. 1). Second, the gate–source capacitance C_{GS} nonlinearity is plotted in Fig. 8.

The measured values of C_{GS}, C_{GD}, and C_{DS} were subdivided to model the physical device more properly by separating the junction and parasitic effects. The drain–source conductance was implicitly taken into account by having I_{DS} expressed as a function of V_{DS} as well as V_{GS}. The electron propagation delay of about 6 ps was accounted for by time-delaying the V_{GS} waveform.

Total current waveforms, including dc levels, were monitored at three locations in the amplifier model: 1) under the gate (I_{DS}), 2) in the bond wire connecting the drain of the FET to the output circuit (I_{BONDWIRE}), and 3) in the 50-Ω load at the output (I_{LOAD}). The three waveforms are plotted for the cases of operation below compression (P_{out} = 25.5 dBm) and operation in slight compression (P_{out} = 29.3 dBm). Below compression (Fig. 9), the current in the FET under the gate did indeed appear quite similar to the class-B half sine wave. In Table I, WATAND's Fourier analysis of I_{DS} gave a second-harmonic level of −17 dBc, a reasonable result considering 1) the slight class-AB biasing and 2) the significant leakage drain current at simultaneous high drain–source voltages and large gate voltages, where the FET should be pinched off and nonconducting. The second harmonic in I_{BONDWIRE} was −27.8 dBc, indicating considerable low-pass filtering by C_{DS} at frequencies approaching the device cutoff. I_{LOAD} had second harmonic of −53.4 dBc, to be expected from the filtering of the quarter-wave bias line and the output matching. The second-harmonic content could be increased a few dB by slightly varying the length of the quarter-wave line.

Fig. 10 shows the currents when the output power was increased to 29.3 dBm. The magnitudes of all three waveforms are larger, and clipping distortion is quite evident in I_{DS}. In Table I, the second-harmonic levels dropped in the three currents, while the third harmonic increased about 5 dB. This was reasonable because clipping implies square-wave-type currents that are richer in odd harmonics and poorer in even harmonics.

Beyond illustrating the observed phenomenon of low second-harmonic content in the single-ended amplifiers, the time-domain simulation gave insight into the various filtering mechanisms of the FET and output circuit. Time-domain analysis should prove to be a valuable design tool for large-signal nonlinear microwave circuits.

TABLE I
FOURIER ANALYSIS OF LARGE-SIGNAL TIME-DOMAIN SIMULATION

Fundamental Output Power:		+25.5 dBm	+29.3 dBm	+25.5 dBm	+29.3 dBm
Harmonics:		Second (dBc)		Third (dBc)	
Currents:	I_{DS}	−17	−19.4	−21.6	−16.6
	$I_{BONDWIRE}$	−27.8	−30.3	−26.8	−21.3
	I_{LOAD}	−53.4	−54.8	−32.2	−26.8

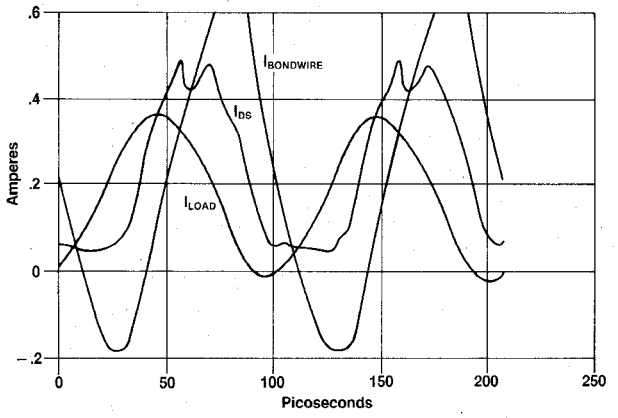


Fig. 10. Current waveforms in simulated circuit ($P_{OUT} = 29.3$ dBm).

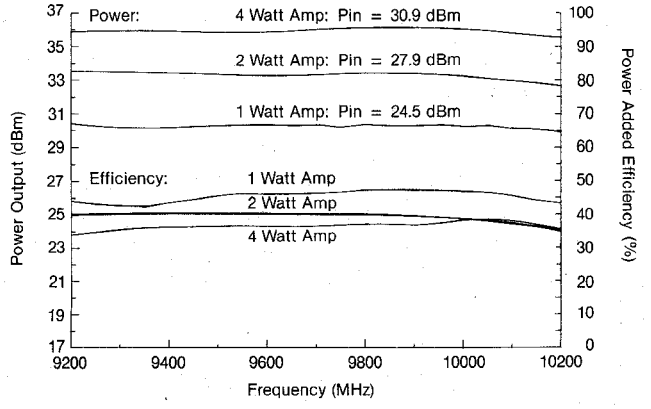


Fig. 11. One-, two-, and four-watt amplifiers: $V_D = 9$ V, $I_{DQ} = 10$-percent I_{DSS}.

VI. PERFORMANCE RESULTS

The measured results are described in three parts.

A. 1-, 2-, and 4-W Individual Amplifiers

This is a direct comparison of optimal 1-, 2-, and 4-W individual amplifiers, each of which was made using high-Q gate-blocking capacitors. The drain voltage of 9 V was used to achieve an output of slightly more than 4 W from the dual push-pull unit, in accordance with the requirements of the sponsoring program, and the 1- and 2-W individual units were biased accordingly.

Fig. 11 gives output power and power-added efficiency versus frequency for the 1-, 2-, and 4-W amplifiers. Roughly, the output power doubles, the gain drops about 0.4 dB, and the efficiency decreases 5 percent at each upward step in the amplifier family. This is attributable

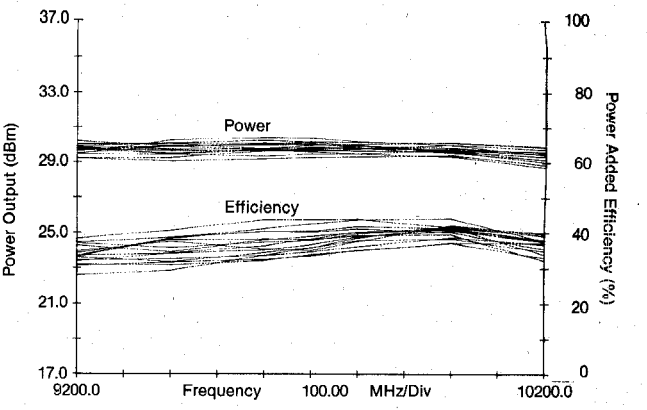


Fig. 12. Power and efficiency of fifteen 1-W amplifiers: $V_D = 8$ V, $I_{DQ} = 10$-percent I_{DSS}, and $P_{in} = 25.1$ dBm.

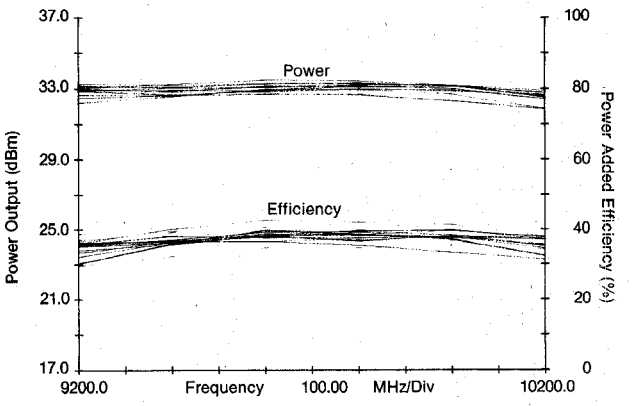


Fig. 13. Power and efficiency of fifteen 2-W amplifers: $V_D = 8$ V, $I_{DQ} = 10$-percent I_{DSS}, and $P_{in} = 28.1$ dBm.

mainly to losses in the Wilkinson and/or 0°–180° hybrids used for power combining. The dual push-pull amp had output power of 4.0 to 4.3 W, typically with 5-dB gain and 35-percent power-added efficiency in the 9.2–10.2-GHz band. All three amplifier plots were made at about the 1-dB gain compression point; the drain current drawn under RF drive (quiescent current $I_{DQ} = 10$-percent I_{DSS}) was 45–50-percent I_{DSS}.

B. 1-W and 2-W 15-Unit Performance

The performance of lots of 15 of the 1-W and 2-W amplifiers is presented to emphasize the repeatability and the consistency of the design. All 30 of the amplifiers initially contained the low-Q gate-blocking capacitors discussed in Section II; after discovering the impact of their lossiness, capacitors of higher Q were retrofitted into the fifteen 1-W amps. Since the 2-W push-pull topology inherently eliminates two of these components, the smaller gain and efficiency improvement anticipated by installing high-Q capacitors in those units was judged unnecessary. The drain voltage was set at 8 V in all 30 amplifiers in order to simultaneously maximize efficiency and meet the output power specifications of the sponsoring program.

Figs. 12 and 13 show the measured output power and power-added efficiency of the 1-W single-ended and 2-W push-pull groups across the 9.2–10.2-GHz band. The ret-

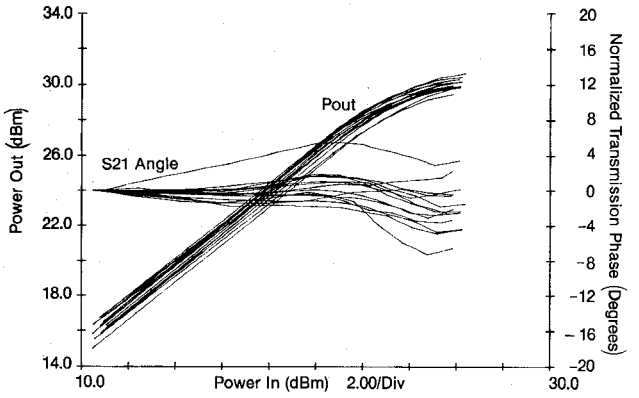


Fig. 14. Output power and transmission phase of 15 1-W amplifiers. Frequency = 9600 MHz.

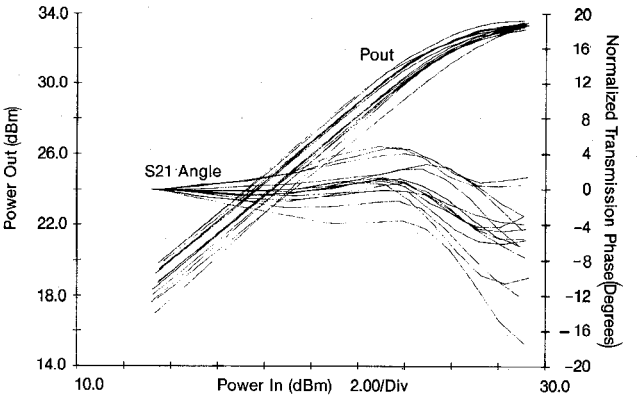


Fig. 15. Output power and transmission phase of 15 2-W amplifiers. Frequency = 9600 MHz.

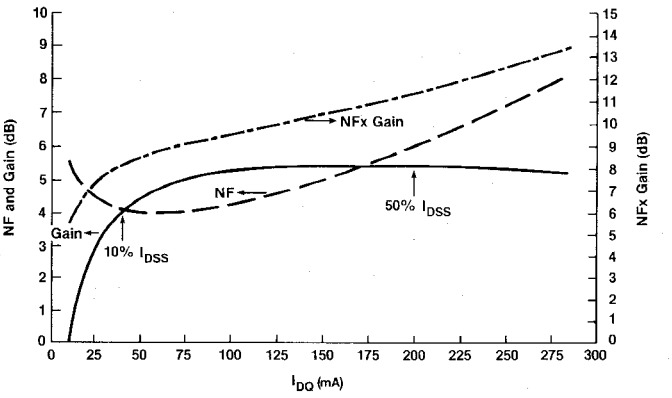


Fig. 16. Small-signal gain and noise figure of 1-W single-ended amplifier.

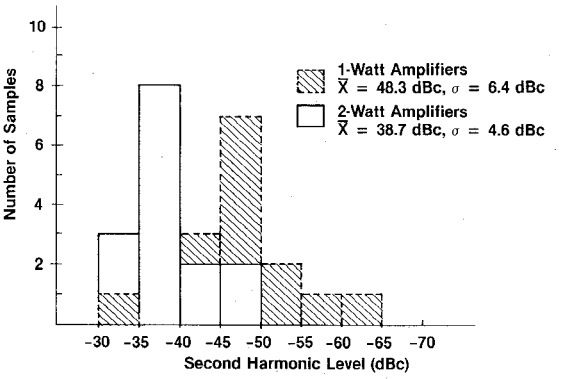


Fig. 17. Superimposed histogram of second-harmonic levels of 1- and 2-W amplifers. Input frequency = 9600 MHz.

rofit of the high-Q capacitors in the 1-W amplifiers had increased their average midband efficiency by 5 percent, to 38 percent, and the gain improved 0.7 dB. At 9.7 GHz, the standard deviations of the output power and efficiency were 0.29 dBm and 1.88 percent for the 1-W single-ended lot and 0.22 dBm and 1.86 percent for the 2-W push-pull lot.

Figs. 14 and 15 give both output power and the transmission phase shift (normalized to the small-signal transmission phase) versus input power for the 1- and 2-W groups. Note that the phase distortion was generally low until gain compression of the amplifiers became significant, giving low AM-to-PM conversion at rated power. The capacitor retrofit had also improved the 1-W amplifier phase distortion characteristics.

It is to be emphasized that once the prototype tuning had been done for each type of amplifier, there was no tuning needed on any of the 30 units fabricated to obtain the consistency of performance exhibited by Figs. 12–15. There were no extra or rejected amplifiers built.

C. Noise Figure and Distortion Measurements

Noise Figure: The noise figure for both the single-ended and push-pull amplifiers was at least 1.5 dB lower at the 10-percent I_{DSS} operating point than at 50-percent I_{DSS}. Noise figure and small-signal gain are plotted for one of the 1-W single-ended amplifiers versus bias current in Fig. 16; the smaller resulting gain–noise figure product can be taken as an index of lower amplifier noise generation when idling.

AM-to-PM Conversion: The normalized transmission phase versus input power data, presented graphically in Figs. 14 and 15, were used to calculate the worst-case average AM-to-PM conversion. For the 15 1-W units, the slope of the phase was generally worst in the +22 dBm to +24 dBm input power range; here, the mean AM-to-PM conversion was −0.62°/dB, with a standard deviation of 0.45°/dB. For the +25 dBm to +27 dBm input range, the 15 2-W amplifiers showed a mean conversion of −1.80°/dB and a standard deviation of 0.56°/dB.

Second-Harmonic Content: Measurements were made of the second-harmonic content of each of the 15 single-ended and 15 push-pull amplifiers at rated power levels using a 9.7-GHz input signal. The results, shown in the superimposed histogram of Fig. 17, indicate that the second-harmonic output is well below the fundamental output, with a mean suppression of −48.3 dBc in the 1-W units (6.4-dBc standard deviation) and a mean of −38.7 dBc (4.6-dBc standard deviation) for the 2-W amplifiers. The higher average second harmonic in the 2-W units was caused at least partially by the necessity of driving them about 0.5 dB proportionally harder than the 1-W ampli-

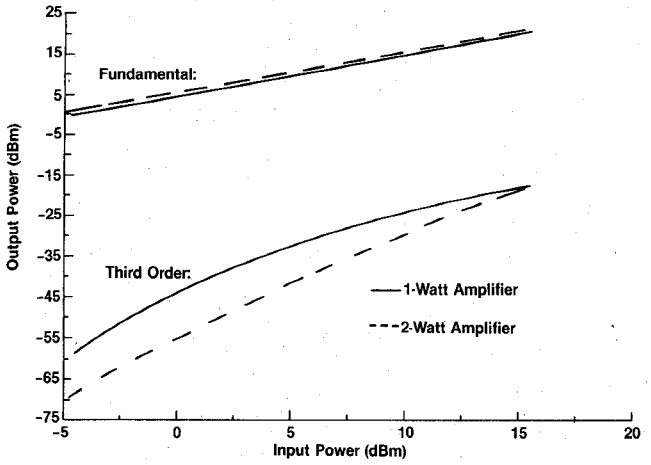


Fig. 18. Two-tone third-order intermodulation products for 1- and 2-W amplifiers.

fiers to achieve rated power; this was because the push-pull amplifiers still contained the low-Q gate capacitors. Interestingly, the phase lengths of the 0°–180° push-pull hybrids could be adjusted to give slightly less than −60-dBc second-harmonic levels at a single frequency.

Intermodulation Products: Extensive testing was not done on the two-tone intermodulation performance of the high-efficiency amplifiers. However, two-tone tests on one single-ended and one push-pull amplifier were run. Fig. 18 plots the two-tone fundamental and third-order product power levels to about the +23-dBm output power level, or 7 dB to 10 dB below rated power. At small-signal input levels (less than −4.0 dBm for the 1-W amplifier and less than −1.0 dBm for the 2-W one), the single-ended amplifier's third-order intercept power was 28.7 dBm, and the push-pull's was 36.4 dBm, values only slightly above and below the output power ratings, respectively. These intercept power points would thus be useful for calculating intermodulation products at output power levels 30 dB or more below rated power.

VII. Conclusions

The results of this effort have demonstrated the high power-added efficiency obtainable in microwave FET power amplifiers by biasing at drain currents approaching pinchoff (10-percent I_{DSS} here) instead of the more common 50-percent I_{DSS} value of class-A operation. A time-domain computer simulation of a 1-W amplifier design permitted visualization and analysis of the nonlinear output currents and showed the progressive harmonic filtering effects of the FET drain–source parasitics and output matching.

A dual push-pull amplifier gave greater than 4.0-W output, 35-percent power-added efficiency, and 5.0-dB gain in the 9.2–10.2-GHz band. The data for lots of 15 1- and 2-W amplifiers showed the repeatability and consistency of performance that is needed for many power amplifier applications. Finally, measurements showed that AM-to-PM conversion, second harmonics, and third-order intermodulation products were low, and that the noise figure benefited from the lower bias current.

Acknowledgment

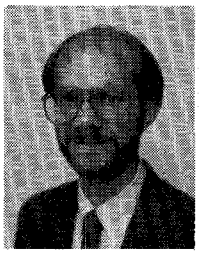
R. A. Neidhard and R. E. Neidert were the AFWAL and NRL Contract Monitors, respectively. P. A. Stenger designed the Wilkinson splitter, and D. C. Boire designed the 0°–180° hybrid. W. J. Fennell and W. F. Stortz fabricated and tested the amplifiers and characterized the chips.

References

[1] R. G. Freitag, J. E. Degenford, and M. Cohn, "High efficiency single-ended and push-pull class B FET power amplifiers," presented at the 1985 GOMAC Conference (Orlando, FL), Nov. 1985.

[2] M. Cohn, J. E. Degenford, and R. G. Freitag, "Class B operation of microwave FETs for array module applications," in *1982 MTT Symp. Dig.*, pp. 169–71.

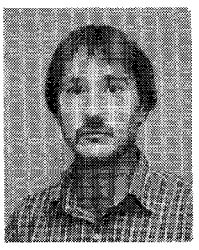
[3] S. March, "A wideband stripline hybrid ring," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-16, p. 361, June 1968.



John R. Lane (M'86) was born in Dayton, OH, on May 3, 1951. He received the B.S.E. degree in electrical and mechanical engineering in 1975 and the M.S. degree in electrical engineering in 1976, both from Duke University, Durham, North Carolina. He has done additional graduate work at the University of Maryland.

From 1976 to 1979, he was employed by Westinghouse Advanced Technology Laboratories, Baltimore, MD. He was a member of the Technical Staff at COMSAT Laboratories, Clarksburg, MD, from 1979 to 1981. In 1981, he rejoined Westinghouse, where he is currently in the GaAs Technology Group. He was program manager of the 4-watt amplifier effort presented as part of this paper. His design experience includes power and low-noise amplifiers, FET mixers and attenuators, and passive components.

Mr. Lane served on the 1986 MTT-S Symposium Technical Program Committee. He is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Eta Sigma.

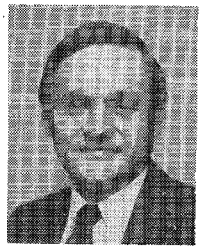


Ronald G. Freitag (S'76–M'77) was born in Baltimore, MD, on August 21, 1956. He received the B.S. degree in electrical engineering from Virginia Polytechnic Institute and State University in 1977 and the M.S. degree in electrical engineering from the University of Maryland, College Park, in 1985.

In 1977, he joined the Microwave Circuit Development Group at Westinghouse Electric Corp., Baltimore, MD, where he worked on various hybrid and monolithic MIC designs and component modeling. In 1984, he joined the GaAs Technology Group, where is is currently involved in MMIC amplifier and millimeter-wave detector design. He was the designer of the one- and two-watt high-efficiency amplifiers reported in this paper.

Hyo-Kun Hahn (M'77) was born in Seoul, Korea, on December 16, 1943. He received the B.S.E.E. degree from Lehigh University, Bethlehem, PA, in 1966 and the Ph.D. degree in electrical engineering from Johns Hopkins University, Baltimore, MD, in 1973.

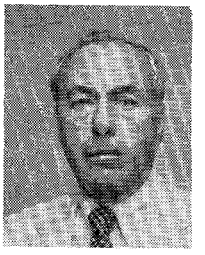
His professional career began with Xerox Corporation in the electronic typesetting R&D group. He joined Westinghouse in 1976, with interests in analog circuit design and analysis. His experience includes radar systems analysis, UHF oscillator design and SAW devices, and GaAs digital logic. More recently, he has been involved with distributed amplifier design and the simulation of nonlinear GaAs microwave devices and circuits, including the time-domain analysis presented here. His present interest lies in two-dimensional numerical analysis of semiconductor devices.



James E. Degenford (S'59–M'64–SM'85–F'86) was born in Bloomington, IL, on June 11, 1938. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1960, 1961, and 1964, respectively.

His work as a graduate student and Research Associate at the University of Illinois was in the fields of millimeter- and submillimeter-wave transmission systems and detection techniques. In 1965, he joined Westinghouse Electric Corporation, working in microwave integrated circuits with emphasis on image-enhanced mixers and low-noise amplifiers. Since 1979, he has been involved in the areas of monolithic GaAs FET amplifiers and monolithic microwave integrated circuits and currently is manager of the GaAs Technology Laboratory.

Dr. Degenford is past chairman of the Baltimore MTT-S chapter and past finance chairman of the MTT-S Administrative Committee. He is listed in American Men of Science and is a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and Sigma Tau.



Marvin Cohn (S'49–A'51–M'57–SM'61–F'74) was born in Chicago, IL, on September 25, 1928. He received the B.S. and M.S. degrees in electrical engineering from the Illinois Institute of Technology, Chicago, in 1950 and 1953, respectively, and Dr. Eng. from Johns Hopkins University, Baltimore, MD, in 1960.

From 1951 through 1969, he was with the following organizations: the Martin Company, the Radiation Laboratory of Johns Hopkins University, and the Advanced Technology Corporation, all of Baltimore. Dr. Cohn is currently a Senior Management Scientist at Westinghouse Advanced Technology Division, in Baltimore. He has directed programs on low-noise circuits, millimeter-wave components and subsystems, power amplifiers, and GaAs devices and MMIC's.

Dr. Cohn is a past member and secretary–treasurer of the MTT-S Administrative Committee and was the chairman of the 1986 International Microwave Symposium Technical Program Committee.